

RELIABILITY DATA LTC6812 & LTC6813 PCN

7/12/2019

• Operating Life Test

PACKAGE TYPE	SAMPLE SIZE	OLDEST DATE CODE	NEWEST DATE CODE	K DEVICE HOURS AT +125°C	NUMBER OF FAILURES
LQFP	154	1916	1916	25.87	0
	154			25.87	0

• Early Life Failure Rate Test

PACKAGE TYPE	SAMPLE SIZE	OLDEST DATE CODE	NEWEST DATE CODE	K DEVICE HOURS AT +125°C	NUMBER OF FAILURES
LQFP	800	1916	1916	38.40	0
	800			38.40	0

1. Electro-Static Discharge (ESD) Test Results

1.1 Test Description

The HBM ESD testing was performed on a THERMOFISHER Mk.2 using the Human Body Module per JESD22-A114. This test is performed for classification only. **Class 1A >±250V, Class 1B >±500V, Class 1C >±1000V, Class 2 >±2000V, Class 3A >±4000V and Class 3B >±8000V.** A copy of the circuit is shown below:

1.2 Test Circuit & Condition

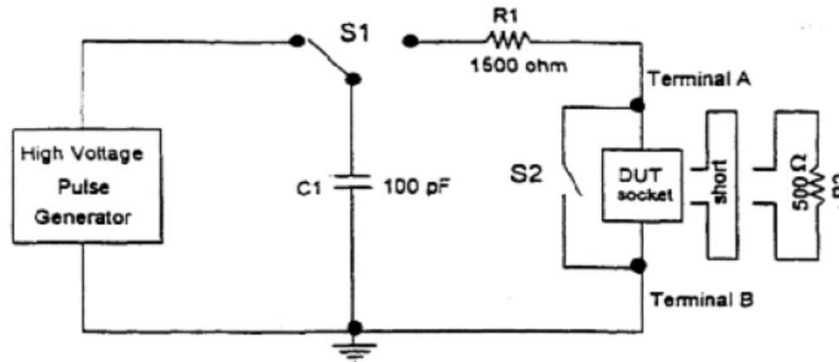


Figure 1 — Typical equivalent HBM ESD circuit

NOTE 1 The performance of any simulator is influenced by its parasitic capacitance and inductance.

NOTE 2 Precautions must be taken in tester design to avoid recharge transients and multiple pulses.

NOTE 3 R2, used for initial equipment qualification and requalification as specified in 3.1, shall be a low inductance, 4000 V, 500 Ω resistor with +/-1% tolerance.

NOTE 4 Stacking of DUT socket adaptors (piggybacking) is allowed only if the waveforms can be verified to meet the specifications in Table 1.

NOTE 5 Reversal of terminals A and B to achieve dual polarity is not permitted.

NOTE 6 S2 shall be closed at least 10 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state.

NOTE 7 R1, 1500 Ω +/- 1%.

NOTE 8 C1, 100 pF +/- 10% (effective capacitance).

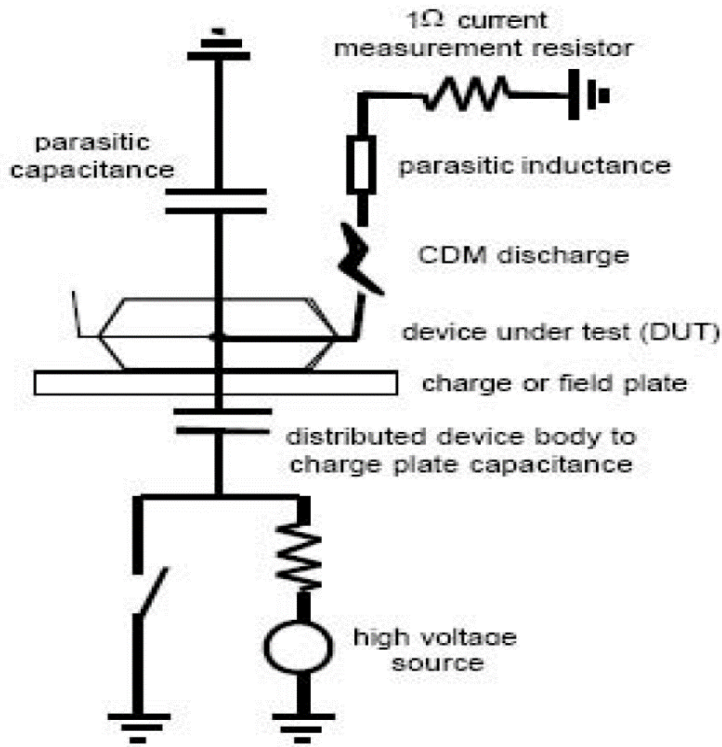
1.3 ESD Data

Device	Model	S/S	Pins	Voltage Passed	Voltage Failed
LTC6813	HBM Class 1C	3	All Pins	>±1000V	

1.7 Test Description

The Charged Device Model (CDM) ESD testing was performed on a THERMOFISHER RCDM system per ESDA ESD STM5.3.1-1999 / AEC-Q100-011-Rev-B. This test is performed for information only. A copy of the circuit is shown below:

1.8 Test Circuit & Condition



(b) Field induced charge CDM

1.9 ESD Data

Device	Model	S/S	Pins	Voltage Passed	Voltage Failed
LTC6813	CDM	3	All Pins	>±750V	

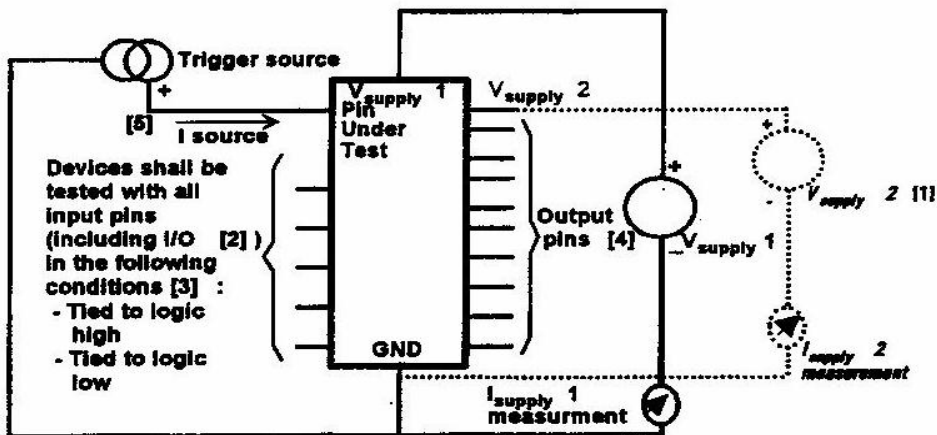
4. Latch-Up Test Results

4.1 Test Description

Latchup Testing was performed at +25°C and +125°C using the LTX Integrated Circuit Test system. The Power Supply pins are biased to the appropriate Datasheet specifications and the individual non-Power Supply pins are tested incrementally while the current is monitored until failure occurs.

4.2 Test Circuit & Condition

4.2.1 Test Circuit 1

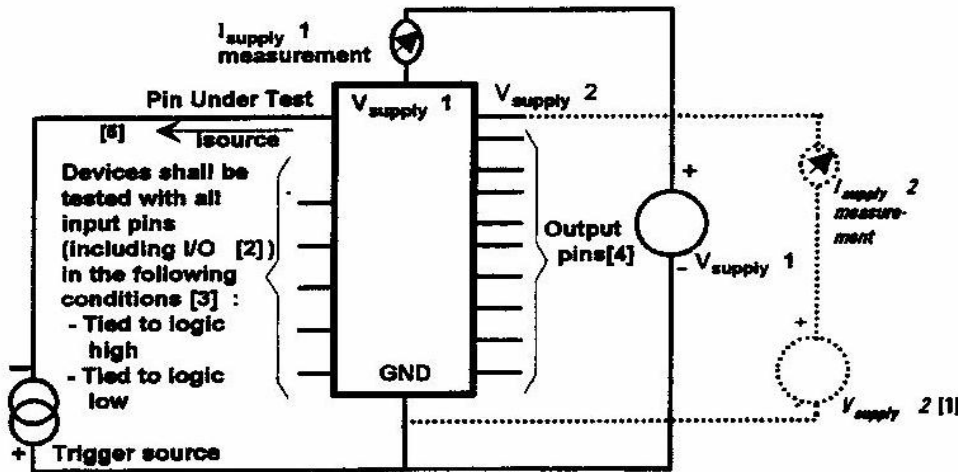


1. DUT biasing shall include additional V_{supply} s as required.
2. DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1. I/O pins in the output state shall be open circuit.
3. Logic high and logic low shall be per the device specification. When logic levels are used in respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.
4. Output pins shall be open circuit except when latch-up tested.
5. The trigger test condition is defined in figure 2 and table 1.

NOTE: Dynamic devices may have timing signals applied per 4.2.3.

Figure 5 - The equivalent circuit for positive input/output I-test latch-up testing

4.2.2 Test Circuit 2



1. DUT biasing shall include additional $V_{supplies}$ as required.
2. DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1. I/O pins in the output state shall be open circuit.
3. Logic high and logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification, unless these conditions violate the device setup condition requirements.
4. Output pins shall be open circuit except when latch-up tested.
5. The trigger test condition is defined in figure 3 and table 1.

NOTE: Dynamic devices may have timing signals applied per 4.2.3.

Figure 6 - The equivalent circuit for negative input/output I-test latch-up testing

4.3 Latch-Up Data

Device	Mode	Current	Temp	S/S	Results
LTC6813	CKT1 & CKT2	>±200mA	+25°C	5	PASS
	CKT1 & CKT2	>±100mA	+125°C	5	PASS

LTC6813 PCN Datasheet Changes

LTC6813-1

	MIN (OLD)	MIN (NEW)
t_{CYCLE}	2027	1743
	352	303
	2717	2337
	174.2	150.0
	29.1	25.0
	232.3	200.0
	970	834
	176	151
	1307	1124
t_{SKEW1}	168	144
	470	404
t_{SKEW2}	202	174
	580	500

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
ADC Timing Specifications							
t_{CYCLE} (Figure 3, Figure 4, Figure 6)	Measurement + Calibration Cycle Time When Starting from the REFUP State in Normal Mode	Measure 18 Cells	●	2027	2343	2488	μs
		Measure 3 Cells	●	352	407	432	μs
		Measure 18 Cells and 2 GPIO Inputs	●	2717	3140	3335	μs
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Filtered Mode	Measure 18 Cells	●	174.2	201.3	213.8	ms
		Measure 3 Cells	●	29.1	33.6	35.7	ms
		Measure 18 Cells and 2 GPIO Inputs	●	232.3	268.5	285.1	ms
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Fast Mode	Measure 18 Cells	●	970	1121	1191	μs
		Measure 3 Cells	●	176	203	215	μs
		Measure 18 Cells and 2 GPIO Inputs	●	1307	1511	1605	μs
t_{SKEW1} (Figure 6)	Skew Time. The Time Difference Between Cell 18 and GPIO1 Measurements, Command = ADCVAX	Fast Mode	●	168	194	206	μs
		Normal Mode	●	470	543	577	μs
t_{SKEW2} (Figure 3)	Skew Time. The Time Difference Between Cell 18 and Cell 1 Measurements, Command = ADCV	Fast Mode	●	202	233	248	μs
		Normal Mode	●	580	670	711	μs

